

FIG. 1

20

FRAMER FARM

24

SIGNALING QUEUE

SIGNAL REGISTER

26

DS1/E1

DS1/E1

DS1/E1

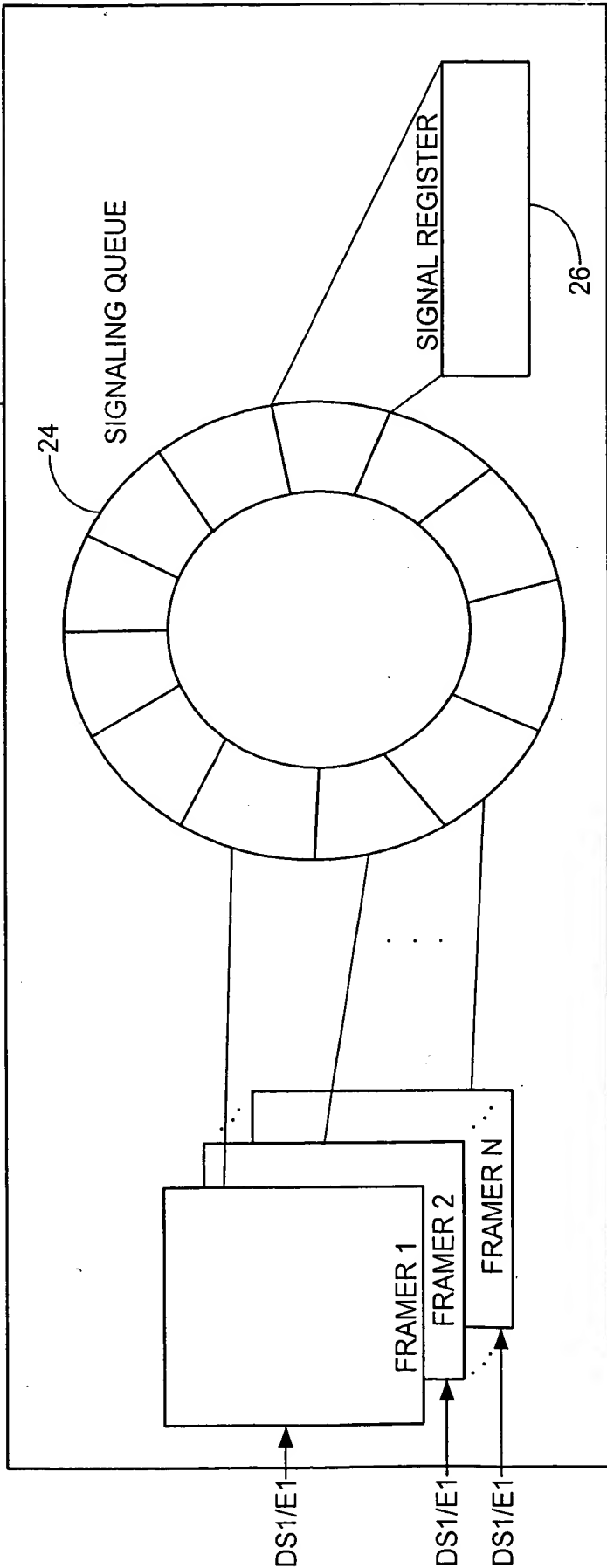
FRAMER 1

FRAMER 2

FRAMER N

FRAMER FARM WITH N DS1/E1 FRAMER

FIG. 2



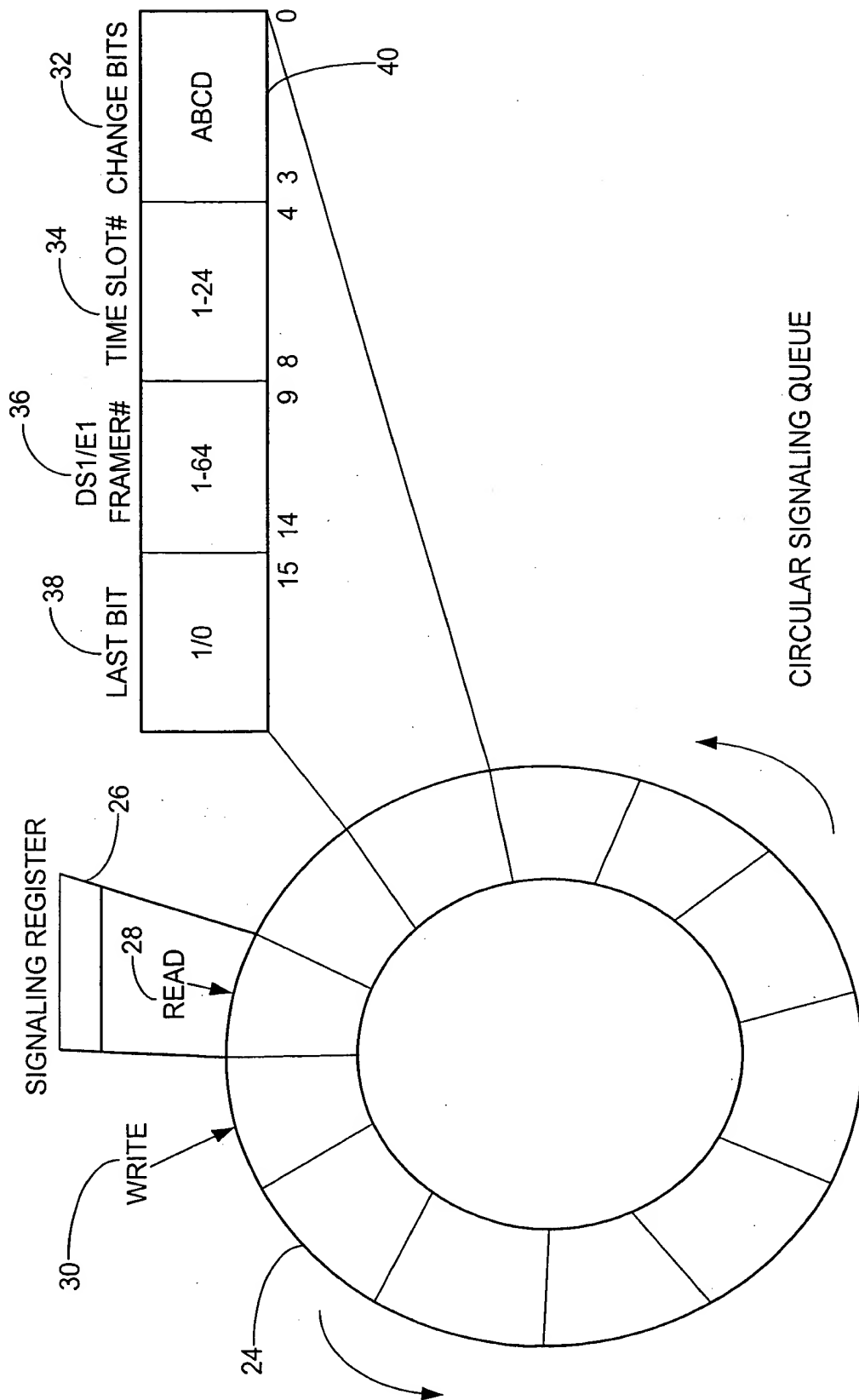


FIG. 3

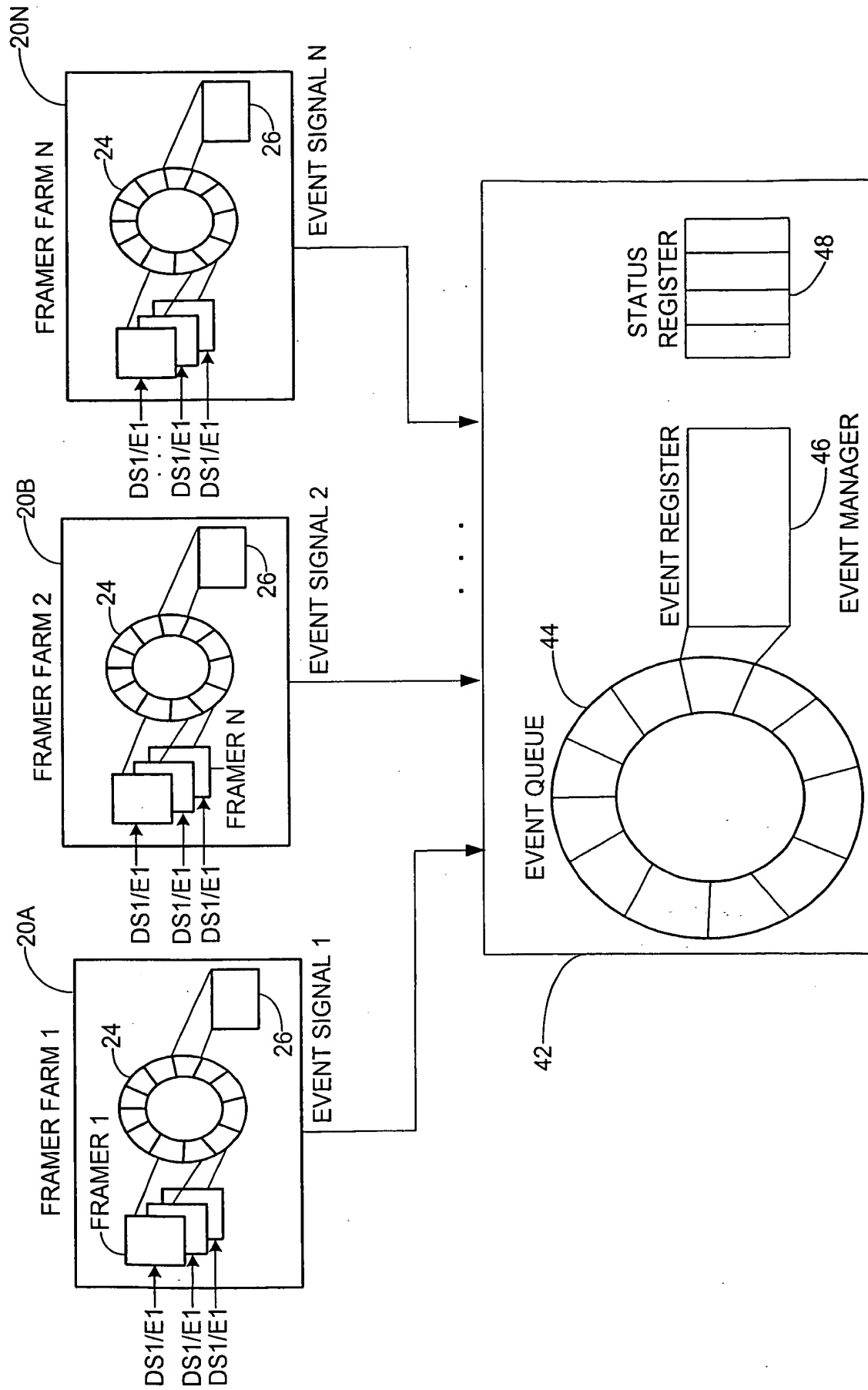


FIG. 4

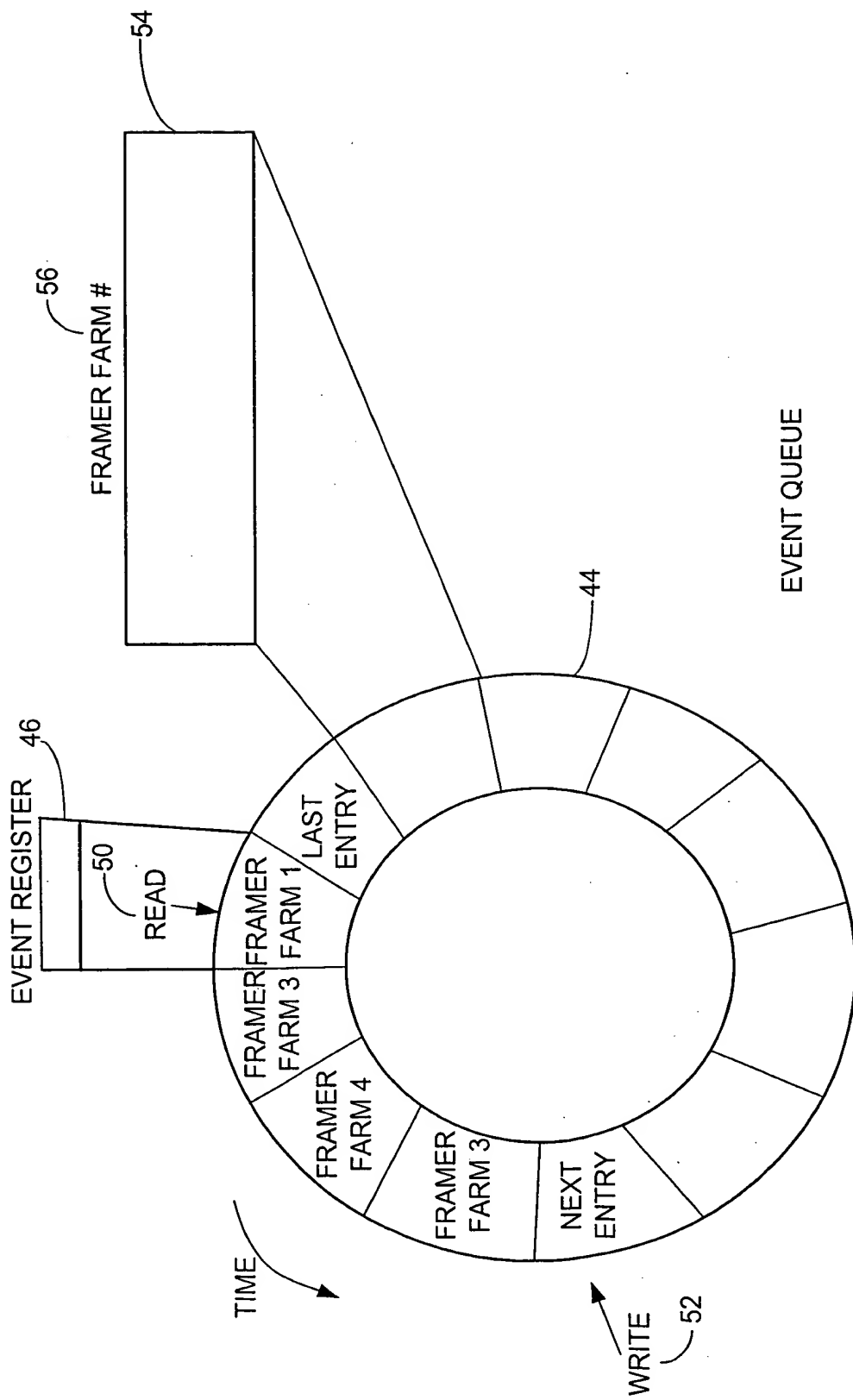


FIG. 5A

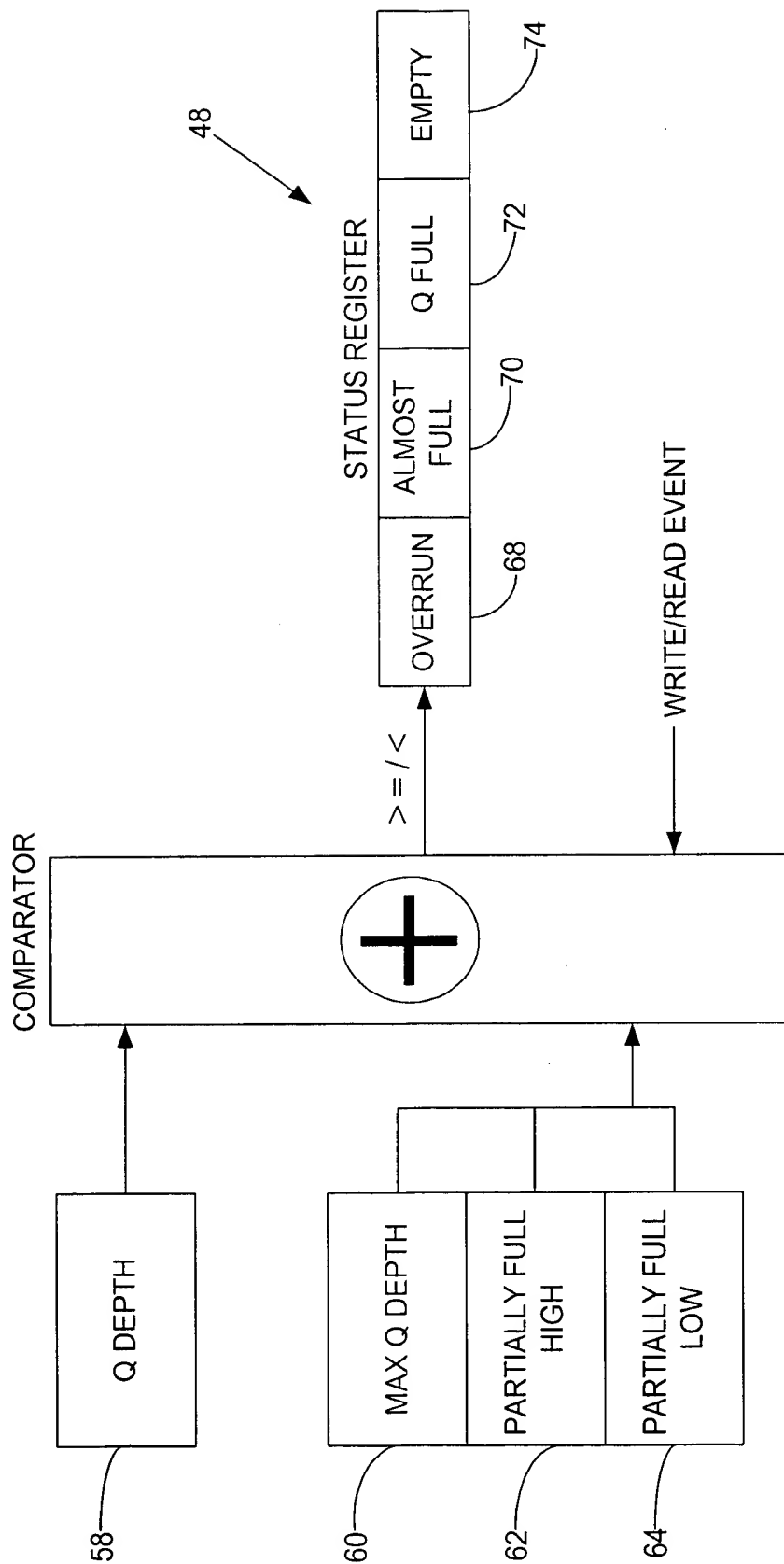


FIG. 5B

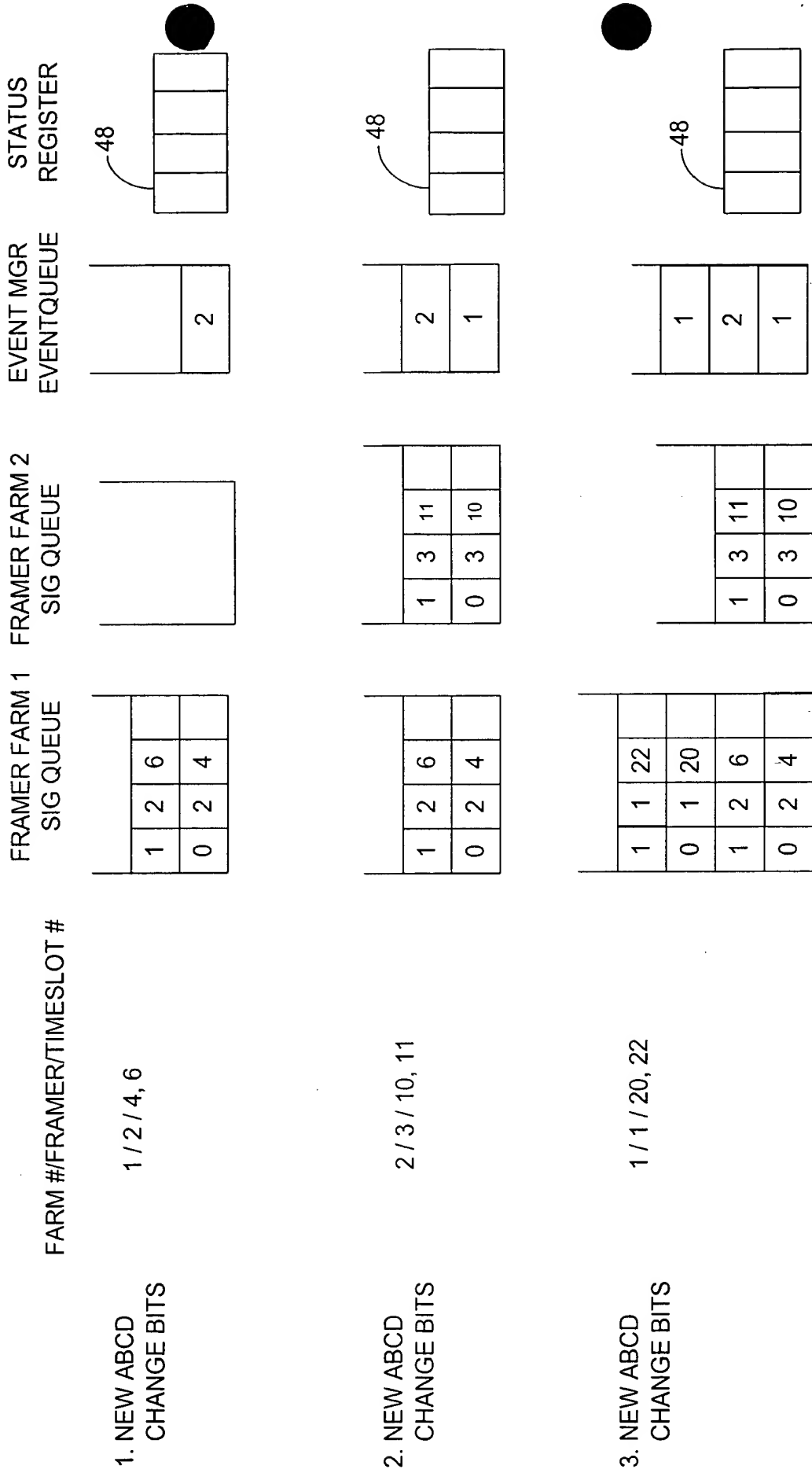


FIG. 6A

4. MICROPROCESSOR PROCESSES EVENTS

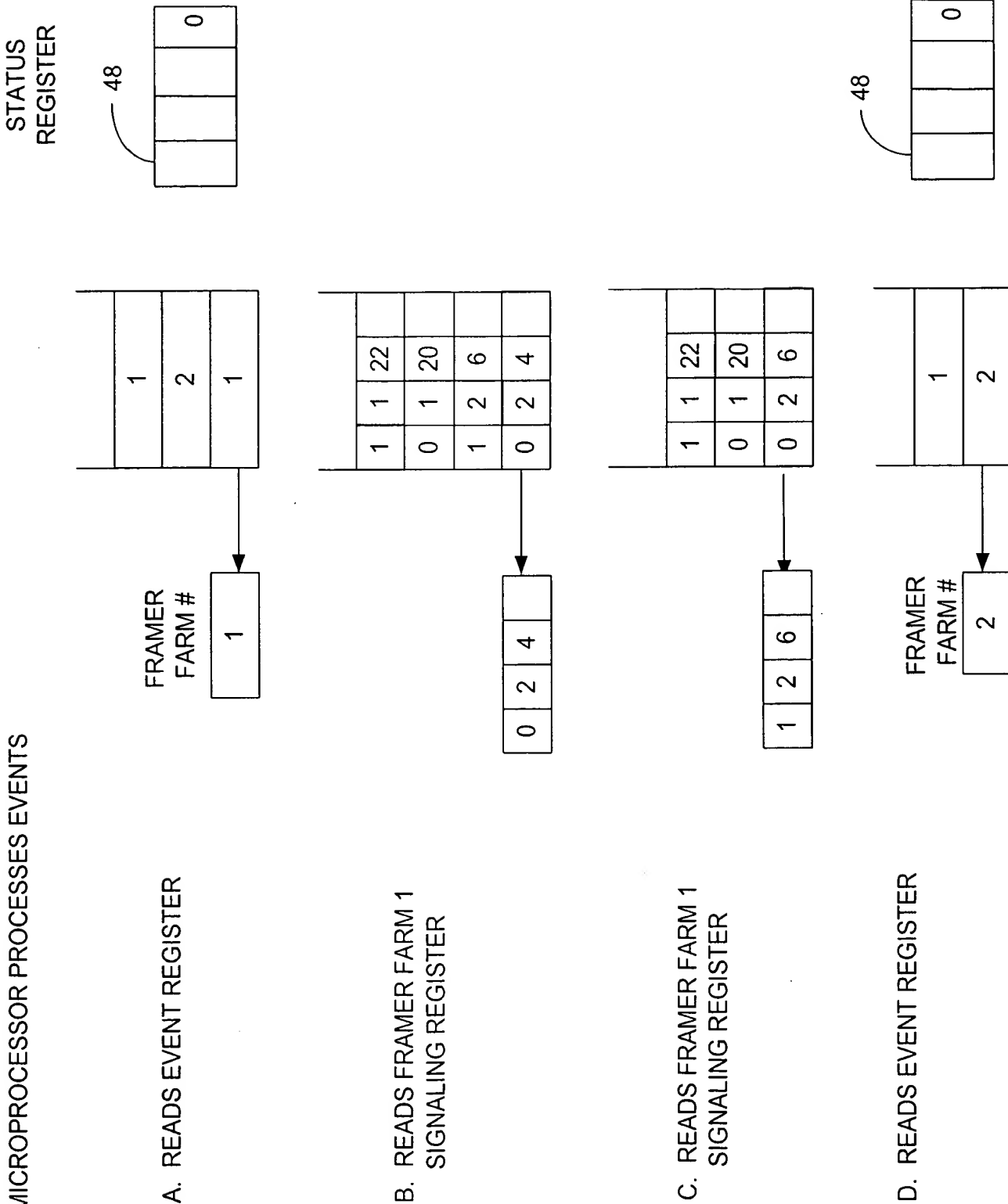
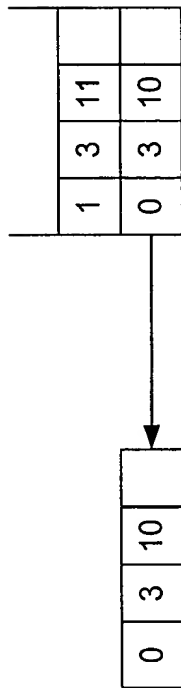


FIG. 6B

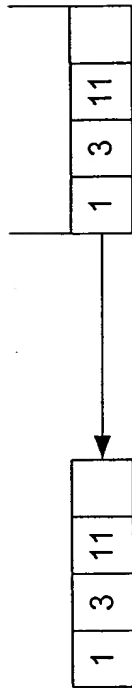
STATUS
REGISTER

4. MICROPROCESSOR PROCESSES EVENTS

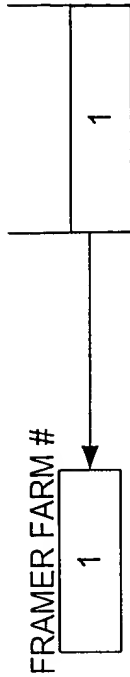
E. READS FRAMER FARM 2
SIGNALING REGISTER



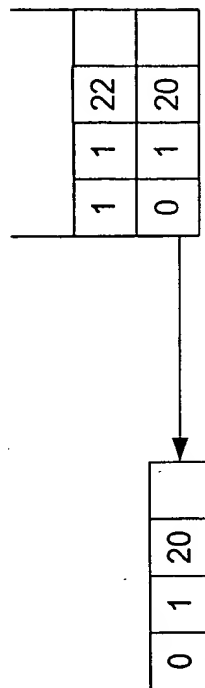
F. READS FRAMER FARM 2
SIGNALING REGISTER



G. READS EVENT REGISTER



H. READS FRAMER FARM 1
SIGNALING REGISTER



I. READS FRAMER FARM 1
SIGNALING REGISTER

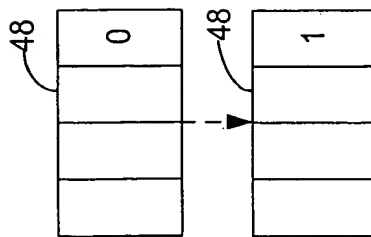


FIG. 6C

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1/2/6

2/3/10

2/3/11

1/1/20

1/1/22

FIG. 7

FRAMER FARM 1
SIGNALING QUEUE

FRAMER FARM 2
SIGNALING QUEUE

1

1	2	6	
0	2	4	

2

1	2	6	
0	2	4	

1	3	11	
0	3	10	

3

1	1	22	
0	1	20	
0	2	6	
0	2	4	

1	3	11	
0	3	10	

FIG. 8

PROCESSOR

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1 / 2 / 6

1 / 1 / 20

1 / 1 / 22

2 / 3 / 10

2 / 3 / 11

FIG. 9

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